Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**.019”**

**.019”**

**.005”**

**.0045”**

**.003”**

**.003”**

**Top Material: Al**

**Backside Material: Au**

**Bond Pad Size = .003 x .004” min.**

**Backside Potential: COLLECTOR**

**Mask Ref: SKL**

**APPROVED BY: DK DIE SIZE .019” X .019” DATE: 4/1/19**

**MFG: ALLEGRO/SPG THICKNESS .007” P/N: 2N5088**

**DG 10.1.2**

#### Rev B, 7/1